WHAT IS CLAIMED IS:

1. A memory cell comprising:

a body region doped with charge carriers of a first type;

a source region disposed in the body region, the source region doped with charge carriers of a second type; and

a drain region disposed in the body region, the drain region doped with charge carriers of the second type,

wherein the body region and the source region form a first junction, wherein the body region and the drain region form a second junction, and wherein a conductivity of the first junction from the body region to the source region in a case that the first junction is unbiased is substantially less than a conductivity of the second junction from the body region to the drain region in a case that the second junction is unbiased.

2. A memory cell according to Claim 1, further comprising:

a substrate of doped with charge carriers of the first type,

wherein the body region is disposed within the substrate.

3. A memory cell according to Claim 2, wherein the substrate is more heavily doped than the body region.

4. A memory cell according to Claim 1, further comprising:

a halo implant disposed in the body region, the halo implant doped with charge carriers of the first type, the halo implant and the drain region to form at least a portion of the second junction.

5. A memory cell according to Claim 4, wherein the halo implant is more heavily doped than the body region.

6. A memory cell according to Claim 1, further comprising:

a trench adjacent to the body region to separate the body region from an adjacent memory cell.

7. A method to write a value to a memory cell, comprising:

forward-biasing a first junction formed by a body region of the memory cell, the body region doped with charge carriers of a first type, and a drain region disposed within the body region, the drain region doped with charge carriers of a second type, to eject charge carriers of the first type from the body region,

wherein a source region disposed in the body region is doped with charge carriers of the second type and is coupled to ground,

wherein the body region and the source region form a second junction, and

wherein a conductivity of the second junction from the body region to the source region in a case that the second junction is unbiased is substantially less than a conductivity of the first junction from the body region to the drain region in a case that the first junction is unbiased.

8. A method according to Claim 7, wherein the memory cell comprises a halo implant disposed in the body region, the halo implant doped with charge carriers of the first type, the halo implant and the drain region to form at least a portion of the first junction.

9. A method according to Claim 8, wherein the halo implant is more heavily doped than the body region.

10. A method according to Claim 7, wherein the memory cell comprises a trench adjacent to the body region to separate the body region from an adjacent memory cell.

11. A method to write a value to a memory cell, comprising:

operating the memory cell in saturation to inject charge carriers of a first type into a body region of the memory cell, the body region doped with charge carriers of the first type,

wherein a drain region disposed within the body region is doped with charge carriers of a second type,

wherein a source region disposed in the body region is doped with charge carriers of the second type and is coupled to ground,

wherein the body region and the source region form a first junction,

wherein the body region and the drain region form a second junction, and

wherein a conductivity of the first junction from the body region to the source region in a case that the first junction is unbiased is substantially less than a conductivity of the second junction from the body region to the drain region in a case that the second junction is unbiased.

12. A method according to Claim 11, wherein the memory cell comprises a halo implant disposed in the body region, the halo implant doped with charge carriers of the first type, the halo implant and the drain region to form at least a portion of the second junction.

13. A method according to Claim 12, wherein the halo implant is more heavily doped than the body region.

14. A method according to Claim 11, wherein the memory cell comprises a trench adjacent to the body region to separate the body region from an adjacent memory cell.

15. A method to read a value stored by a memory cell, comprising:

operating the memory cell in a substantially linear operational region to develop a drain current based on a number of charge carriers of a first type that are disposed in a body region of the memory cell, the body region doped with charge carriers of the first type,

wherein a drain region disposed within the body region is doped with charge carriers of a second type,

wherein a source region disposed in the body region is doped with charge carriers of the second type and is coupled to ground,

wherein the body region and the source region form a first junction,

wherein the body region and the drain region form a second junction, and

wherein a conductivity of the first junction from the body region to the source region in a case that the first junction is unbiased is substantially less than a conductivity of the second junction from the body region to the drain region in a case that the second junction is unbiased.

16. A method according to Claim 15, wherein the memory cell comprises a halo implant disposed in the body region, the halo implant doped with charge carriers of the first type, the halo implant and the drain region to form at least a portion of the second junction.

17. A method according to Claim 16, wherein the halo implant is more heavily doped than the body region.

18. A method according to Claim 15, wherein the memory cell comprises a trench adjacent to the body region to separate the body region from an adjacent memory cell.

19. A method according to Claim 15, further comprising:

determining the stored value based on the drain current.

20. A system comprising:

a microprocessor comprising a memory cell, the memory cell comprising:

a body region doped with charge carriers of a first type;

a source region disposed in the body region, the source region doped with charge carriers of a second type; and

a drain region disposed in the body region, the drain region doped with charge carriers of the second type,

wherein the body region and the source region form a first junction, wherein the body region and the drain region form a second junction, and wherein a conductivity of the first junction from the body region to the source region in a case that the first junction is unbiased is substantially less than a conductivity of the second junction from the body region to the drain region in a case that the second junction is unbiased; and

a double data rate memory coupled to the microprocessor.

21. A system according to Claim 20, the memory cell further comprising:

a halo implant disposed in the body region, the halo implant doped with charge carriers of the first type, the halo implant and the drain region to form at least a portion of the second junction.

22. A system according to Claim 21, wherein the halo implant is more heavily doped than the body region.

23. A system according to Claim 20, further comprising:

a trench adjacent to the body region to separate the body region from an adjacent memory cell.